Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **INPUT**
2. **COMMON**
3. **OUTPUT**

**.088”**

**.069”**

**2**

**1**

**3**

**MASK**

**REF**

**7**

**8**

**0**

**5**

**A**

**Top Material: Al**

**Backside Material: Ti/Ni/Ag**

**Bond Pad Size: .004” X .004”**

**Backside Potential: COMMON**

**Mask Ref: 7805A**

**APPROVED BY: DK DIE SIZE .069” X .088” DATE: 4/27/23**

**MFG: TEXAS INSTRUMENTS THICKNESS .014” P/N: UA7805**

**DG 10.1.2**

#### Rev B, 7/1